0-30 VDC Input

ESD Protection

Isolated enable for analog frontend

Create isolated split supply (+/-12 VDC @ +/-85 mA max.) (Switching Freq: 5 to 20 MHz)

Remove switch-reg. noise

Low-noise +/-5V rails for analog frontend.

D1 SMBJ30CA

R1 33k

DVPOS

VBAT+

U3 TPC817S1D

VBAT-

R4 1.2k

Vf=~1.2 @ If=3mA

U2 IM2412S (+VIN, EN, NC, -VIN, +VOUT, COM, -VOUT)

+12V

-12V

AGND

L1 NFZ32BW881HN10L

L3 NFZ32BW881HN10L

C1 1uF

R2 (TBD)

R3 (TBD)

C6 1uF

U1 ADP7118AUJZ (VIN, EN, SENSE/ADJ, VOUT, GND)

C2 100nF

C4 100nF

C3 4.7uF

C5 4.7uF

L2 NFZ32BW101HN11L

L4 NFZ32BW101HN11L

AVPOS

AVNEG

U4 ADP7182AUJZ-5.0 (VIN, EN, GND, VOUT, NC)

N_AFE_EN

J1 43650-1001

1 EXT_5VDC
2 EXT_GND
3 CTRL_SCL
4 CTRL_SDA
5 TEMP_SCL
6 TEMP_SDA
7 N_TEMP_INT
8
9 VBAT+
10 VBAT-

Thu-hole R/A header
MicroFit3.0
plastic support pegs
gold finish

DN1 PESD5V0U4BW

DN2 PESD5V0U4BW

ESD Protection

DVPOS

DGND

External off-board always-on 5V digital supply.

Bus pull-ups

DVPOS

R13 10k

Populate only one pull-up when multiple !ALERT outputs (from different boards in a stack) are bussed together.

Bus (dis)connect configuration

R5 (TBD)

R6 (TBD)

CONTROL_SCL

CONTROL_SDA

JMP1 DNP

JMP2 DNP

JMP3

JMP4

DVPOS

R7 (TBD)

R8 (TBD)

TSENSOR_SCL

TSENSOR_SDA

N_TSENSOR_ALERT

J2 CON10

J3 CON10

1 EXT_5VDC
2 EXT_GND
3 CTRL_SCL
4 CTRL_SDA
5 TEMP_SCL
6 TEMP_SDA
7 N_TEMP_INT
8
9 VBAT+
10 VBAT-

Board-Stacking Connectors

ASSEMBLY NOTES:
* Use solder paste containing RMA flux. Do not use no-clean or water-soluble types.
* Wash board for 15min in clean IPA & hexanes, then bake for 1.5hours at 125 deg. C. (for RMA flux)
* Populate address-selection switches AFTER board washing; they may not stand up to vigorous washing; consider them splash-proof, but nothing more.
* Populate J3 for triaxial/3-pin photodiodes or J4 for coaxial/2-pin photodiodes.
* To CONNECT the bias circuit, populate R19 & R21 and remove R20. Use the reverse configuration to run without the bias circuit.
* Install shields after washing.
* Populate/Omit I2C pull-ups and their values according to system bus capacitance and speed.
* Battery & I/O connectors' shroud mating face must be <= 5.5mm from board edge.

Mounting Holes (Clearance)
For use with plastic 21mm M3 standoffs
(Essentra Components' CBMFTS310A)

MP1 M3 MP2 M3 MP3 M3 MP4 M3

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Title: **Photodiode Analog Frontend - ALTAIR Project**

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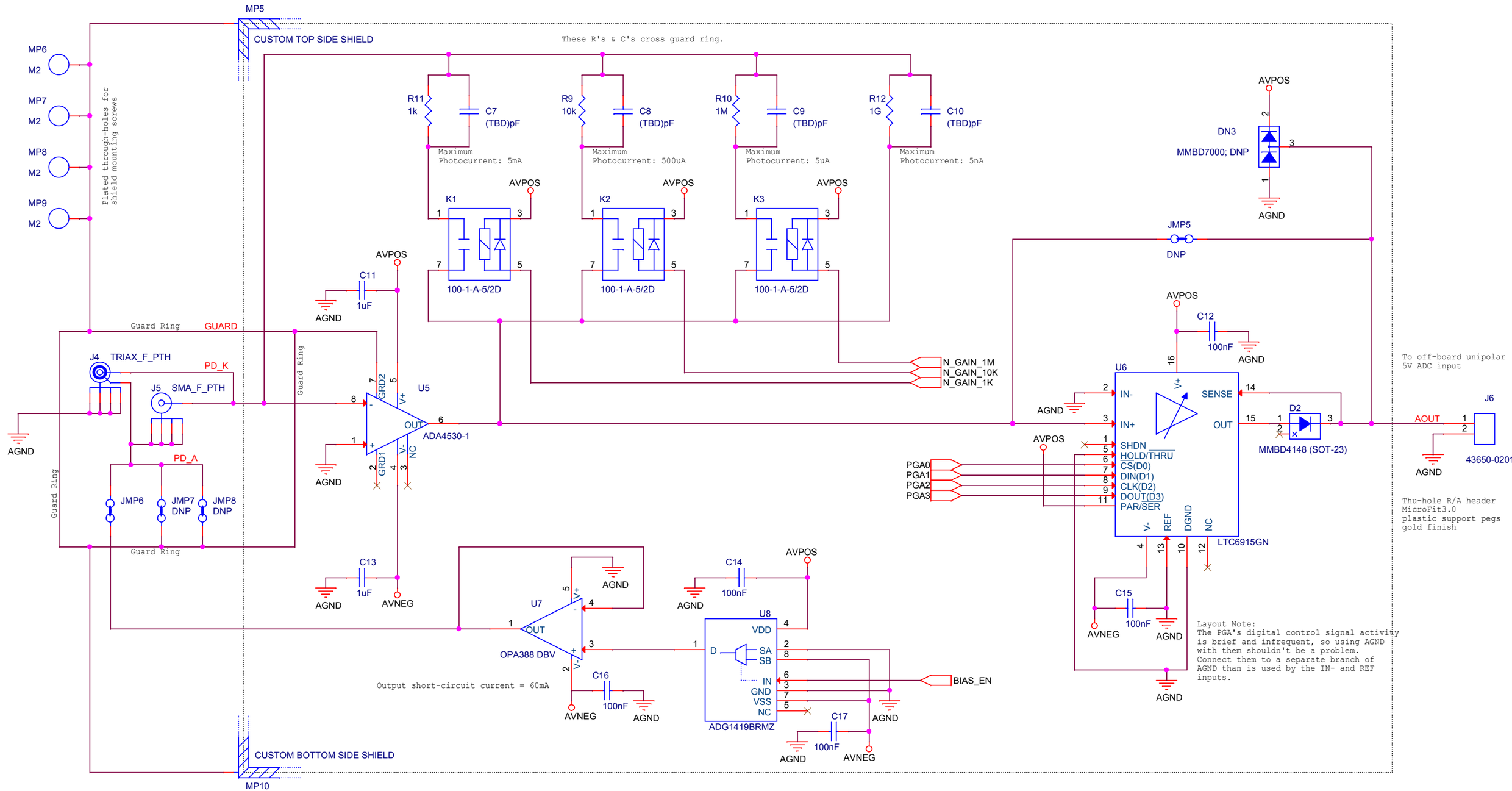
Preamp:
* Relay-controlled gain settings are the parallel combination of both the switched and hardwired R's & C's.
* Guard ring surrounds the input trace and is driven to the same potential to reduce PCB leakage errors.
* Photodiode must not see any parasitic electrical connections through its mounts!
* Feedback capacitor values (marked TBD--to be determined) must be tuned for the specific photodiode to be used. Use C0G/NP0 ceramic capacitors or better.

Reed Relays:
* 1TOhm isolation min., low thermal EMF
* Drive current is ~2mA @ 5V. Any thermal EMF may produce a drifting offset as the relay slowly self-heats.
* Coil pins must be placed OUTSIDE guard ring

Gain Stage:
* For each of the 1k, 10k, 1M and 1G transimpedance gain ranges, the PGA provides gains of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, and 4096. The total number of gain settings is 52.
* The RRIO ideal-diode output protects ADC from under-range output voltages.
* Jumper zerohm resistor R1 provides a simple means of bypassing the PGA if it's not needed. If populating R1, depopulate the PGA (U8) and/or diode (D4).



Reverse-Bias Control:
* Meant to improve linearity at higher photocurrents
* When bias is not applied, the bias circuit drives the diode anode to AGND potential (ideally equal to guard potential) to maintain guard ring integrity. The OPA388's upper-rail input & output capability and ultra-low offset help ensure this.
* Bias puts -5V on diode coaxial connector shield, so insulation is required!!!
* Do not short coaxial connnector shield to AGND or use it as a reference for circuit measurements!!

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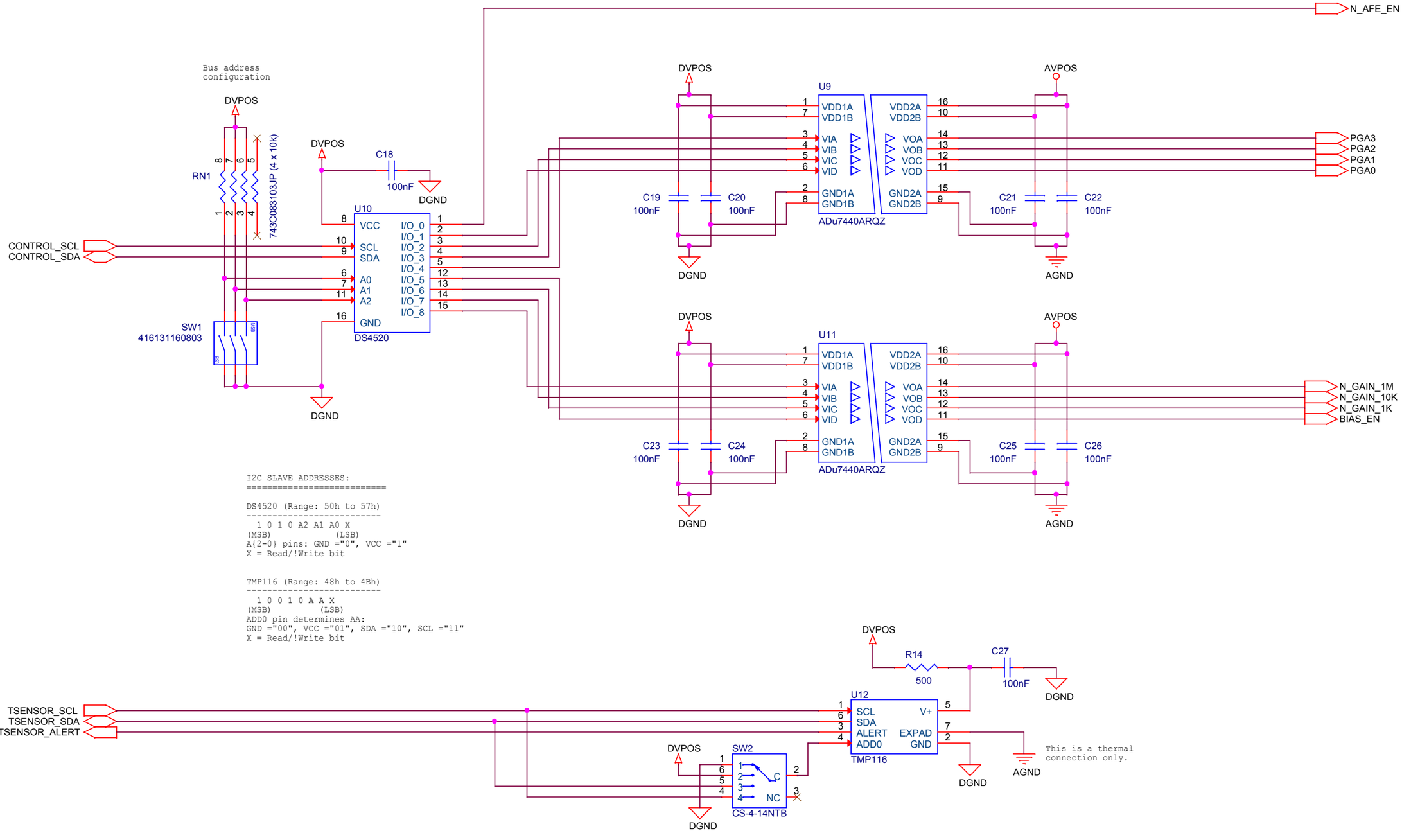

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