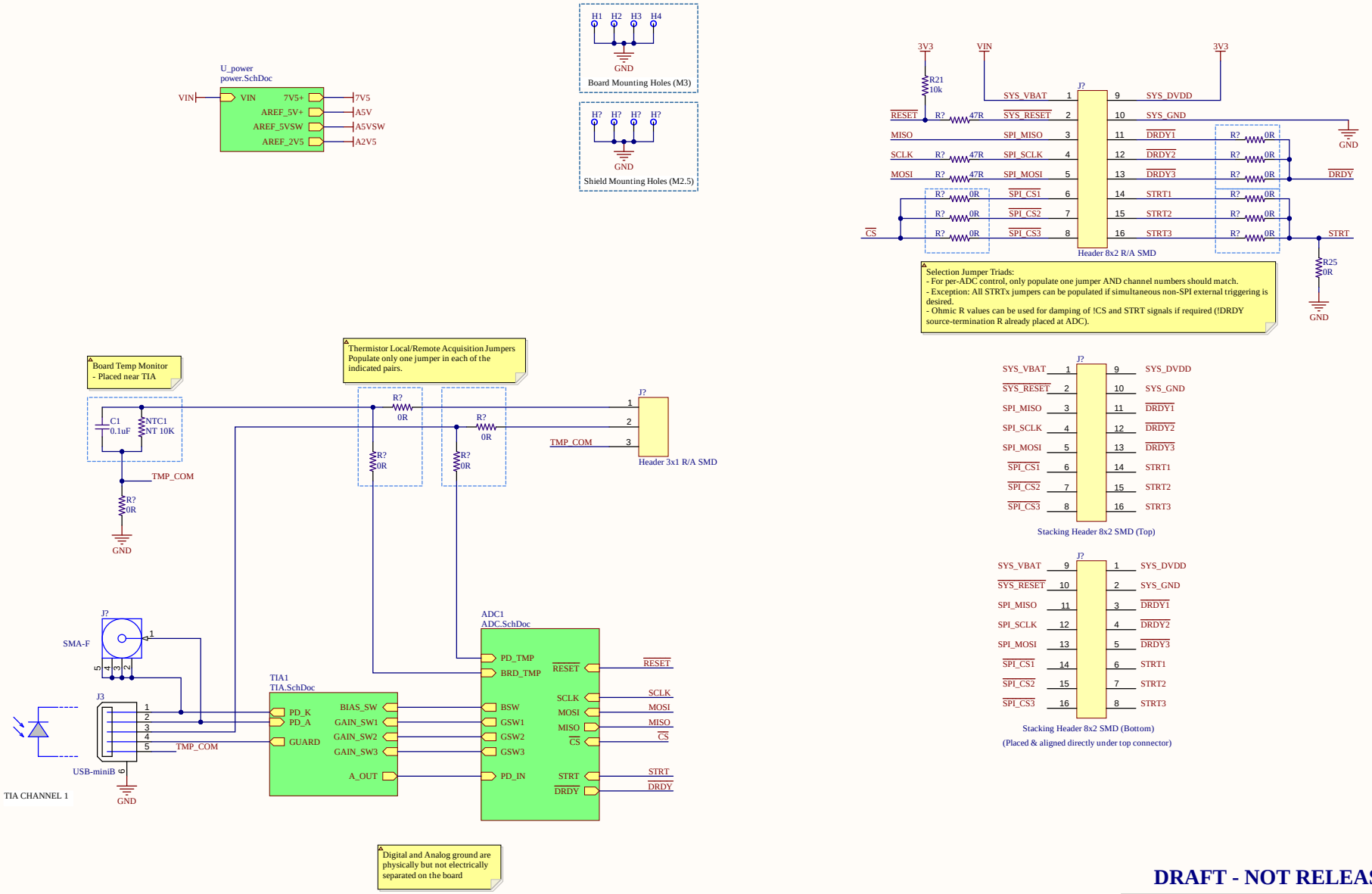
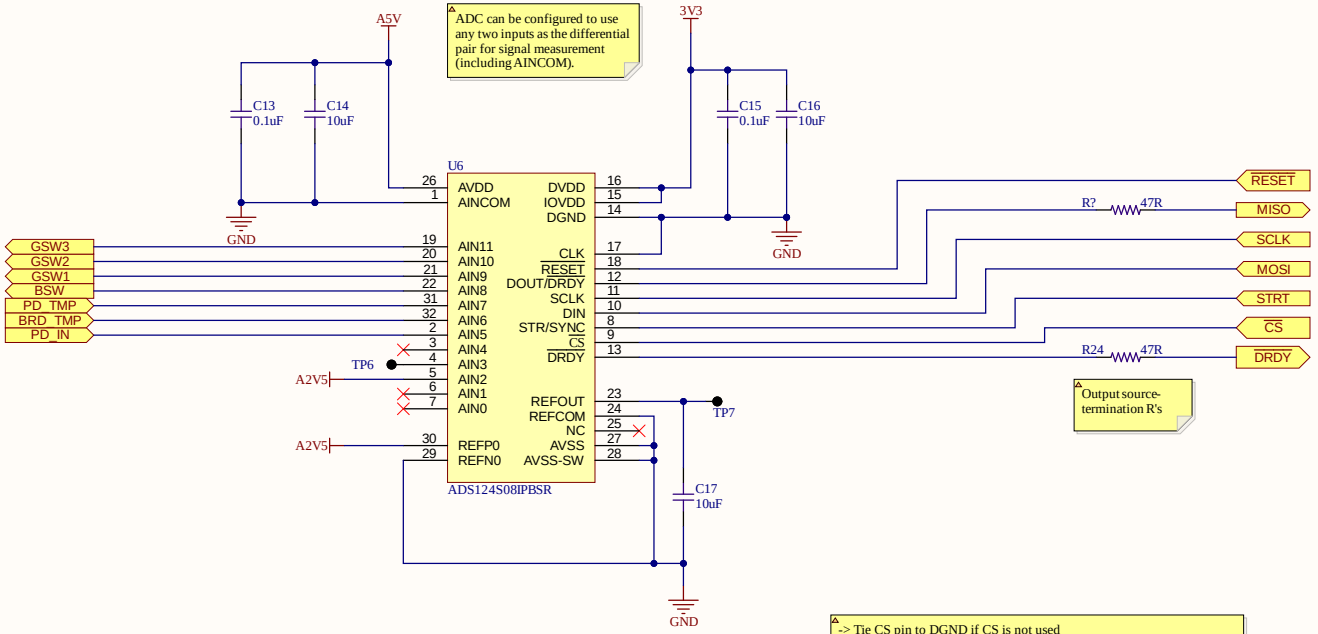

U_power
power.SchDoc
VIN
7V5+
AREF_5V+
AREF_5VSW
AREF_2V5
7V5
A5V
A5VSW
A2V5
H1 H2 H3 H4
GND
Board Mounting Holes (M3)
H? H? H? H?
GND
Shield Mounting Holes (M2.5)
3V3
VIN
3V3
R21
10k
SYS_VBAT
SYS_DVDD
RESET
R?
47R
SYS_RESET
SYS_GND
MISO
SPI_MISO
DRDY1
SCLK
SPI_SCLK
DRDY2
MOSI
SPI_MOSI
DRDY3
SPI_CS1
STRT1
SPI_CS2
STRT2
CS
SPI_CS3
STRT3
0R
GND
DRDY
STRT
R25
Header 8x2 R/A SMD
Selection Jumper Triads:
- For per-ADC control, only populate one jumper AND channel numbers should match.
- Exception: All STRTx jumpers can be populated if simultaneous non-SPI external triggering is desired.
- Ohmic R values can be used for damping of !CS and STRT signals if required (!DRDY source-termination R already placed at ADC).
Stacking Header 8x2 SMD (Top)
Stacking Header 8x2 SMD (Bottom)
(Placed & aligned directly under top connector)
Board Temp Monitor
- Placed near TIA
C1
0.1uF
NTC1
NT 10K
TMP_COM
Thermistor Local/Remote Acquisition Jumpers
Populate only one jumper in each of the indicated pairs.
Header 3x1 R/A SMD
SMA-F
J3
USB-miniB
TIA CHANNEL 1
TIA1
TIA.SchDoc
PD_K
PD_A
GUARD
BIAS_SW
GAIN_SW1
GAIN_SW2
GAIN_SW3
A_OUT
ADC1
ADC.SchDoc
PD_TMP
BRD_TMP
PD_IN
BSW
GSW1
GSW2
GSW3
Digital and Analog ground are physically but not electrically separated on the board
REV A.6
DRAFT - NOT RELEASED
Title
ALTAIR Photodiode Acquistion Payload
(Based on UVic ORCASat design Rev A.6 by Evan Moore)
Size
Tabloid
Number
Revision
Date: 5-05-2021
File: \\..\top.SchDoc
Sheet of
Drawn By:

ADC can be configured to set A8 - A11 as GPIO. These are used to control the Bias and gain switches for the TIA channels.

AVDD powers the PGA buffer. This requires a 5V rail for our spec to operate correctly. (Max 5.5V)

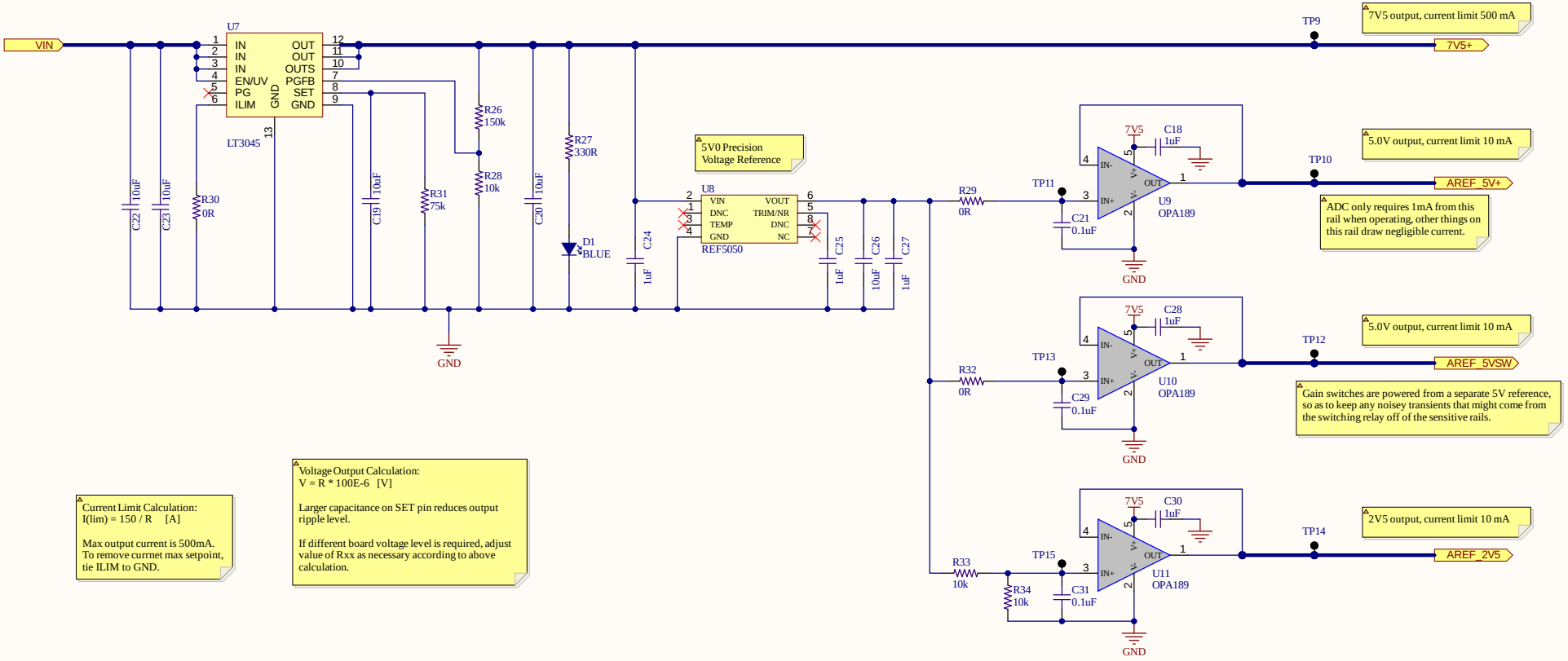
When PGA is bypassed (i.e. in single-ended measurement) the aboslute voltage restrictions on the input are (AVSS - 0.15V) < VIN < (AVDD + 0.15V).

Since the measurement is still a differential one, in order to have access to all possible byte codes (both positive and negative), a differential measurement should be made between the TIA input signal and 2.5V. Therefore when the TIA outputs 5V, the ADC measures a differential signal of 2.5V. And when the TIA outputs 0V (or close to), the ADC measures -2.5V.



REV A.6

Title		
Size: B	Number	Revision
Date: 5-05-2021		Sheet of
File: \\..\ADC.SchDoc		Drawn By:



REV A.6

Title		
Size B	Number	Revision
Date: 5-05-2021		Sheet of
File: \\..\power.SchDoc		Drawn By:

BIAS GENERATOR CALCULATIONS:
Voltage Output Calculation:
V = R * 100E-6 [V]
(Resistance at SET pin)

Use trimmer pot for ground testing to adjust voltage setpoint.

For flight, populate SET resistor with appropriate value, and remove trimmer pot. SET resistor should be low drift.

Larger capacitance on SET pin reduces output ripple level.

Current Limit Calculation:
I(lim) = 150 / R [A]
(Resistance at ILIM pin)

Max output current is 500mA. To remove currnet max setpoint, tie ILIM to GND.

GAIN SWITCHING

GAIN_SW3
GAIN_SW2
GAIN_SW1

A5VSW
J?
J5
U?
U1
R? 47R
R? 100k
R9 100k
R? 0R
R6 0R
R? 1k
R? 10k
R8 1M
K? 100-1-A-5/2D
K1 100-1-A-5/2D
GND

Relay coil resistance 3.3k

Appropriate gain resistor should be at least 1000x less than that of the primary gain resistor

LOGIC HI = Second stage engaged
LOGIC LO = Second stage disengaged

7V5
C2 1uF
C3 0.1uF
C4 1uF
C5 0.1uF

Place caps as close to the V+ terminal of the buffers as possible

Guard trace must be put around the anode signal line

PD_A
GUARD

NOTE: Feedback resistors must have EXTREMELY low thermal drift

Capacitors should have C0G / NP0 rating

R10 1G
C6 220pF

TIA POSITIVE REFERENCE

Voltage divider ensures that even if a small amount of leakage current is present that the TIA will not saturate the ADC.

A5V
R12 10k
TP2
R13 1M
C7 10uF
U3 OPA189
IN+ IN- V+ V- OUT
R11 0R
GND

TRANSIMPEDANCE AMPLIFIER

U2 AD8638
+IN -IN V+ V- OUT
TP3

J6 MMCX
A_OUT

Additional MMCX connector can be used for direct low noise measurement of TIA output

Calculation for primary TIA gain stage resistor:

Resistor value = R [Ohms]
Photosensitivity @ wavelength = p [A/W]
Max incident power on Photodiode = w [W]
Desired headroom at bottom of scale = h [V]
Positive Input Bias = b [V]

R = (b - h) / (p * w)

For p = 0.35 A/W, w = 7.4 mW, h = 0.2 V, and b = 3.3V:
R = 1196.9 Ohms
-> Round to 1.2 kOhms

Calculation for the TIA stability capacitor :

Feedback Resistor Value = R [Ohms] *Caculated above
Bandwidth of Circuit = F [Hz]

C = 1 / (2 * pi * R * F) [F]

For R = 1.2KOhms, and F = 700 kHz:
C = 189 pF

Note that the exact value of the feedback capacitor is largely unimportant, what matters is its order of magnitude.

Even though the output caps are tied directly to the photodiode cathode, they do not unbalance the system. This has been checked in TINA-TI.

PGFB thresh = 0.3 * (1 + R14/R18) + (25nA*R14)

Sets the cutoff voltage for fast startup

BIAS GENERATOR

VIN
U4 LT3045
IN IN IN EN/UV PG ILIM
OUT OUT OUTS PGFB SET GND
R14 249k
R18 10k
R16 0R
R17 91k
C9 10uF
C10 10uF
C11 10uF
C12 10uF
TP4
GND

BIAS SWITCH

Analog signals are limited to VDD + 0.3V, so VDD must be tied to the reverse bias generator output

U5 ADG1419BRMZ-REEL7
SB SA D IN VDD VSS GND NC
C8 1uF
R15 0R
TP5
A5VSW
J7
R19 47R
R20 100k

When "No Bias" is set, the photodiode cathode is connected to the positive input reference of the TIA. The difference in potentials between the cathode and anode of the photodiode then is so small it can be considered negligible.

PD_K
BIAS_SW

LOGIC HI = Reverse photodiode bias engaged
LOGIC LO = No bias on photodiode

REV A.6

Title		
Size: Tabloid	Number	Revision
Date: 5-05-2021		Sheet of
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